SERIES 3500

5½ DIGIT TRIPHASIC™

DIGITAL VOLTMETER

Models 3501, 3502, 3503, 3504, &3505

REFERENCE TECHNICAL DATA

DATA PRECISION

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Chapter 1

INTRODUCTION & SPECIFICATIONS

1.1 GENERAL

The Series 3500 5-½ digit voltmeter is a single-range instrument, available in each of five decade ranges from ±.100000 to ±1000.00 VDC in Models 3501, 3502, 3503, 3504, and 3505, respectively, for the five decades of range scales. Each model in the series features the Tri-phasic™ dual slope automatic zeroing conversion technique with Isopolar referencing on a standard assembly ready for customized or dedicated installations.

Control signals and state-information signals are available through rear-panel connectors for use in automated control, test, and computing systems. Measured values, in BCD format, are outputs through DTL/TTL compatible interface circuits; command and control signals provide the capability for externally or internally triggering measurements according to system needs, and for interfacing with remote printing and display instrumentation.

1.2 SCOPE OF MANUAL

This manual contains the specifications, test data, interface connections, maintenance chart, appropriate schematics, calibration procedure, and combined parts list.

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1.3.1 Performance of Each Model.

CHARACTERISTIC	MODEL 3501	MODEL 3502	MODEL 3503	MODEL 3504	MODEL 3505
FULL SCALE RANGE	±.100000	±1.00000	±10.0000	±100.000	±1000.00
OVERRANGE	±.119999	±1.19999	±11.9999	±119.999	±1000.00
RESOLUTION	1 u Volts	10 u Volts	100 u Volts	1 mV	10 mV
INPUT IMPEDANCE	>1000 MΩ	>1000 MΩ	>1000 MΩ	10 MΩ	10 MΩ
ACCURACY (±1 lsd) 24 hrs. 23° ±1° C)	±0.005% of reading, ±0.004% fs.	±0.004% of reading, ±0.001% fs.	±0.004% of reading, ±0.001% fs.	±0.004% of reading, ±0.001% fs.	±0.004% of reading, ±0.001% fs.
ACCURACY (± 1sd) 6 months, 23° ±5° C)	±0.008% of reading, ±0.004% fs.	±0.007% of reading, ±0.004% fs.	±0.007% of reading, ±0.001% fs.	±0.007% of reading, ±0.001% fs.	±0.007% of reading, ±0.001% fs.
TEMPERATURE COEFFICIENT (0° to 50° C)	±0.001% of reading, ±0.001% fs. per °C	±0.001% of reading, ±0.0002% fs. per °C	±0.001% of reading, ±0.0002% fs. per °C	±0.001% of reading, ±0.0002% fs. per °C	±0.001% of reading, ±0.0002% fs. per °C

1.3.2 Specifications Common to All Models.

ALL MODELS

Maximum Input Voltage: ±1000 VDC

Voltage Coefficient: Add ±0.00001% of reading per volt (affects Models 3504 and 3505 only).

Common-Mode Rejection Ratio
(With 1 KΩ source impedance unbalance)
at DC.....160 dB
at 50 & 60 Hz.....120 DB

Common-Mode Voltage: 300 VDC (peak AC)

Readout: NIXIE™ tubes.

Normal-Mode Rejection Ratio: 60 dB
(at 10 Hz, and all integral multiples of 10 Hz)

INTERFACE AND APPLICATION SPECIFICATIONS

Decimal point....user simply grounds one appropriate pin on rear connector.

Trigger Rate:
Internal.....approx. 3 per sec.
External.....up to 4 per sec.

Control Inputs:
External Trigger.....Positive pulse of 2.4 volts with width > 1μsec and < 100 msec initiates a Read command, causing instrument to perform one measurement. Reading remains in memory until a new external trigger pulse is received.
Trigger Enable: Application of Logic Zero inhibits conversion in all trigger modes.
Logic One.....> 2.4V
Logic Zero.....< 0.4 V Sink for 40 mA

BCD Output (1-2-4-8 BCD Coded, positive true logic):
Logic One.....> +2.4 V
Logic Zero.....< ±0.4 V Sink for 4 mA
Polarity.....Logic one = positive
End of Conversion...Zero to One transition

Input Connector: 5-pin Amphenol miniature connector
(Mating connector is provided.)

ENVIRONMENTAL REQUIREMENTS
Temperature.....Operating: 0° to +50°C
Storage:-25°C to +80°C
Relative Humidity...0° to 40°C:95% max.
+40° to +50°C: 80% max.

POWER REQUIREMENTS: 105-125 VAC or 210-250 VAC, 47-430 Hz, 10W. (Input power selectable by rear-panel switch). Fuse-protected. Line cord is furnished.

DIMENSIONS: 3" H x 8"W x 11" D overall, including PC board and rear bracket.

WEIGHT: 3-1/2 pounds.

STANDARD OPTIONS*
Options are designated by adding option numbers as suffixes to Model Number (e.g., 3502-1-5).

Option 1: 3-wire DC/DC Voltage Ratio Measurements, in addition to DC Voltage Measurements. Accomplished by external connection of 2 of 3 wires. (Specify length of wires required).
Display.....10 x actual ratio
Reference Input.....+1 to ±11VDC 100KΩ impedance
Accuracy and Temperature Coefficient
Standard-model ratings x 10/Ref. voltage
CMRR & NMRR...Same as standard-model ratings for unknown.

Option 2: Same as Option 1, except Reference Input Impedance = 1MΩ

Option 3: 4-wire DC/DC Voltage Ratio Measurements, in addition to DC Voltage Measurements. Specifications same as Option 1, except maximum permissible voltage difference between commons is 10 VDC.
Reference Input Impedance.....100kΩ

Option 4: Same as Option 3, except Reference Input Impedance = 1MΩ
Note: Only one of the four preceding options may be ordered.

Option 5: Mating 44-pin connector for BCD outputs + control inputs.

Option 6: Front optical filter.

Option 7: Rack mount kit, including case for installation of Series 3500. Specify left or right side mount.

*For prices & additional information, see Data Precision Brochure #5140-5/75

Chapter 2

INSTALLATION & OPERATION

2.1 GENERAL

The Series 3500 DVM is intended for customized installation as a single-range instrument in the user's measurement system. The basic unit, on its PC-board, may be mounted in the user's case or frame, or, a Data Precision rack-mounting frame (option 7) may be used to adapt the instrument to a standard RETMA 19" rack mounting configuration.

2.2 INSTALLATION

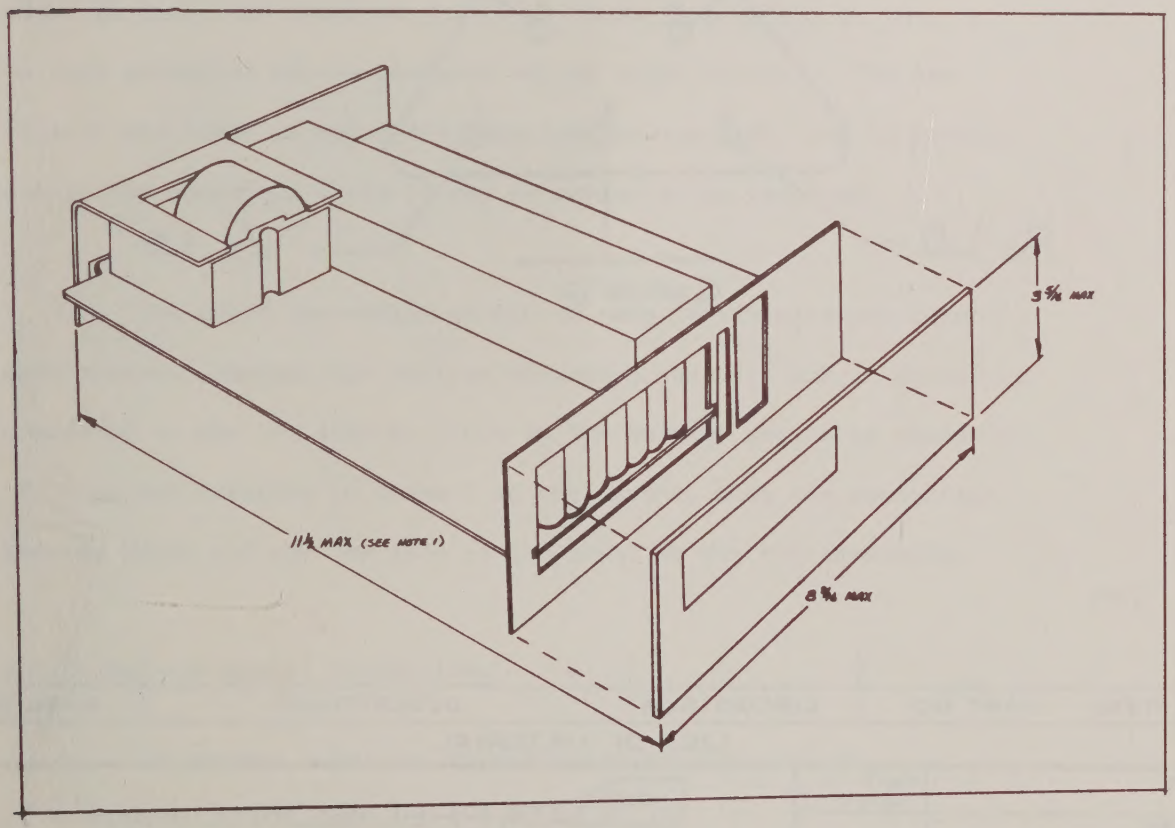
a) Mechanical Interfaces; Outline dimensions and mounting features are identified in the illustration of figure 2-1.

b) Electrical Interfaces; A line-power cord is wired to the Series 3500 power transformer through a rear-panel power-selector switch, providing the user with the option of incorporating the voltmeter in either 115V or 230V AC systems. The input power is fuse-protected. Fuse is mounted on rear panel.

c) Signal Interfaces; Signal input voltages are connected to the meter through a 5-terminal connector mounted on the rear panel; terminal identifications are shown in figure 2-2. The illustration includes the identification of ratio input connections which are applicable when a ratio option is ordered.

d) Control Interfaces; The PC-board connector provides an interface for input control signals and for remote data and display transmissions. Table 2-1 identifies the terminal assignments for this standard 44-pin PC connector, VIKING 2V22D/1-3, or equivalent.

Fig. 2-1 (Dimension Diagram)



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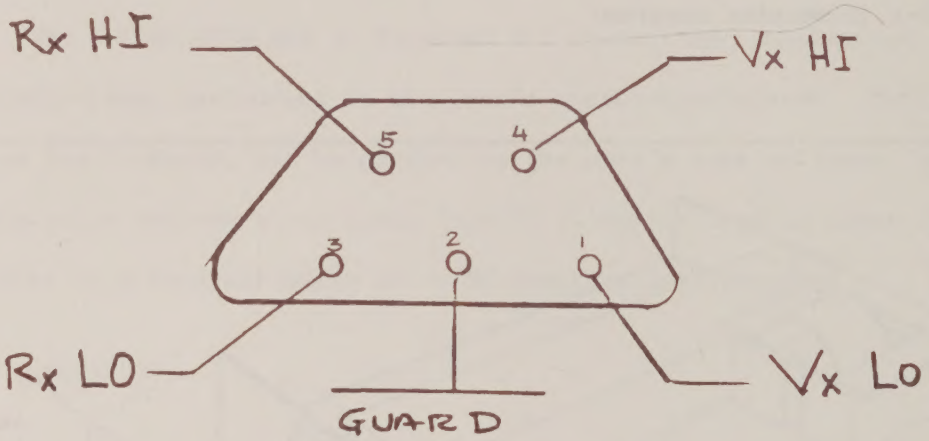
REVISIONS

REV	ECO	DESCRIPTION	DWN	APPLS	DATE

SIZE A

REV



REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

DRAWN	DATE 9/26/75
CHECKED	
DESIGNER	
ENGINEER	
APPROVED	
RELEASED	

DATA PRECISION COMPANY
Data Precision Company, Wakefield, Mass. 01880

SERIES 3500 DIGITAL VOLTMETER
REAR INPUT CONNECTOR

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS ± ANGLES ±

CODE IDENT NO.	SIZE		REV
	A	FIGURE 2-2	
SCALE	ACCOUNT NO.	SHEET	OF

2.3 SIGNAL CONNECTION/MEASUREMENT

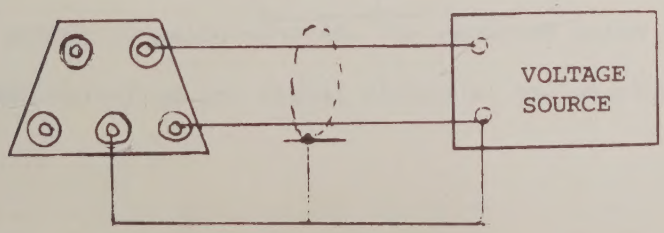
2.3.1 Guard Connections

Instrument construction provides a GUARD circuit connected to the internal shield surrounding the analog and A/D sections of the instrument and isolated from any analog input or external ground. Prior to any measurement, a proper GUARD connection must be made in order to bring the internal shield as close as possible to the voltage potential of the low side of the input circuit. The low side of the input is separated from internal grounds, and is brought out to the connector where it may be connected as required.

The GUARD connection should be made to minimize the common mode currents through the voltage measuring circuit, and it should be connected to the low side as close to the voltage source as possible. If it is not feasible to connect at the source, make the connection between GUARD and the low side of the input at the DVM terminals.

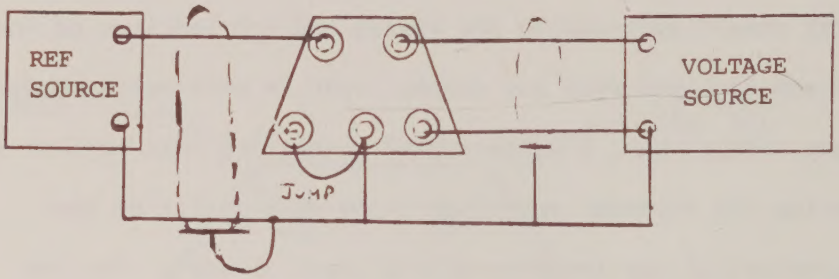
2.3.2 Voltage Signal Connections

See sketch below for signal and guard connections.



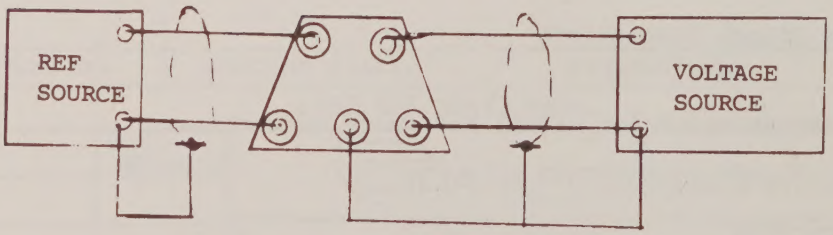
2.3.3 3-Wire Ratio Measurement

If this option is installed, connect signals as shown in sketch.



2.3.4 4-Wire Ratio Measurement

If this option is installed, connect signals as shown in sketch below.



2.4 SIGNAL CONNECTIONS

2.4.1 Set-Up

To obtain remote control and to transmit data from Series 3500 DVM...

Prepare a cable with 44-pin connector VIKING 2VK22D/1-3 or equivalent, and cabled as shown in Table below. Table 2-1

2.4.2 Output Signals Specifications and Applications

a) Data Output - Parallel format of five binary-coded decimal digits and sign are transmitted with DTL/T^2L compatibility. Logic is positive true:

Logic "1" +2.4V

Logic "0" +0.4V sink for 4 mA

Polarity positive is logic "1".

Signals remain as latched on output lines between conversions.

b) Range scale connected is indicated by logic "0".

c) End of Conversion (EOC) is indicated by positive going transition of voltage on output line, at which time (during transition), the data output is being updated. The negative going voltage transition of the READ OUTPUT output signal occurs at the start of conversion in

TABLE 2-1

REMOTE CONTROL/OUTPUT CABLE

A	Ground	1	Ground
B	$\overline{10^1}$ (3503)	2	8
C	8,000	3	4
D	4,000	4	2
E	2,000	5	1
F	1,000	6	NC
H	$\overline{10^0}$ (3502)	7	80
J	Enable	8	40
K	NC	9	20
L	NC	10	10
M	NC	11	$\overline{10^3}$ (3505)
N	800	12	NC
P	400	13	NC
R	200	14	Read Output
S	100	15	80,000
T	$\overline{10^2}$ (3504)	16	40,000
U	NC	17	20,000
V	NC	18	10,000
W	NC	19	100,000
X	$\overline{10^{-1}}$ (3501)	20	+
Y	Overload	21	Ext. Trig.
Z	Ground	22	Ground

Note

See schematic for complete description of signal, identified in same nomenclature as in table. See also Chapter 3 for further discussion of signal waveform and levels.

NC = Not Connected

each measurement cycle and serves as a forewarning of the positive going transition (and upcoming data update) to occur after 100 milliseconds and within 220 milliseconds thereafter.

d) Overload - A zero logic level on this line indicates the input of a signal more than 120% of the full scale range. This output thus serves to indicate existence of incorrect data on the output lines and may be used to inhibit input of incorrect data to receiving printers, computers, etc. It also has a short negative pulse at EOC.

2.4.3 Input Control Signals and Applications

a) In order to exercise external trigger control of DVM measurements, it is necessary to apply a DTL/TTL low level or grounding signal at ENABLE pin J. (See reference Schematic).

b) External Trigger - Application of a 2.4V positive voltage pulse between 1 usec and 100 msec wide at EXT.TRIG pin 21 causes the instrument to initiate the measurement cycle and to update the data output until the next trigger command. The BCD data remains on the output lines between updates, permitting computer processing or printing (logging), and the repetition rate of the external trigger may be adjusted to allow the necessary time between data updates for data receptors to complete their processing (printing, computer input, editing, etc.).

Chapter 3

PRINCIPLES OF OPERATION

3.1 System Block Diagram.

In its simplest form, the Series 3500 DVM is represented by the Block Diagram of Figure 4-1. The system consists of an input Signal Conditioning block, followed by the TRI-PHASIC™ Analog to Digital (A/D) Converter block, whose decoded outputs are driving signals for the Timing and Display block. The Timing & Control block and two Power Supply blocks complete the unit.

The major blocks in Figure 4-1 physically comprise the following:

Analog Block Diagram (Figure 4-2)

Digital Block Diagram (Figure 4-3).

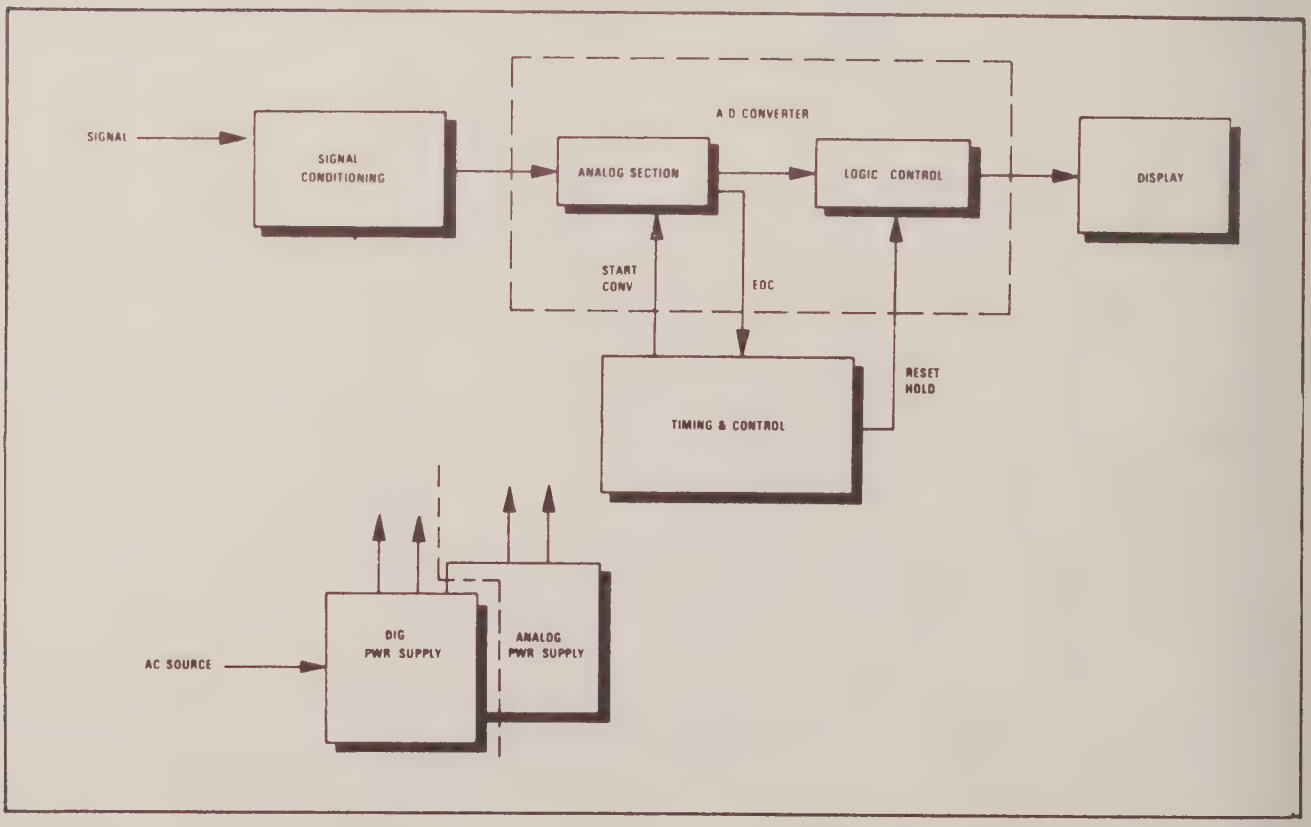


Figure 4-1. Simplified Block Diagram

a) The analog portion of the TRI-PHASIC A/D converter accomplishes the conversion in the three phases of (1) self zeroing, (2) unknown integration, and (3) reference integration, the latter two compensated by the stored value of compensating offset.

As shown in the Analog Block Diagram (Figure 4-2), the DC Volts conditioning block is connected as the input to the A/D preamplifier. The preamplifier output is integrated and then processed by the high gain amplifier. The high gain amplifier outputs: (1) drive the sign indicator at the end of phase 2 to obtain the switching control signals that select the appropriate polarity of the ISO-Polar™ reference voltage to be applied (via the switching network) to the A/D preamplifier in phase 3 and at the same time drive the Display to indicate sign, and (2) indicate end of phase 3. The high gain amplifier in phase 1 also drives the self zeroing circuitry to develop the offset signal to be applied during the phases 2 and 3 as an input to the A/D preamplifier. Logic and Control circuitry in the Analog Block Diagram receive transformer-coupled "trigger" and "start-phase 3" pulses from the Digital Blocks to initiate phase 2 and phase 3 Converter action, respectively, in each conversion cycle and develop end of conversion pulses to be transmitted via transformer coupling to the Digital Blocks to end phase 3. An isolated and triple-shielded Analog Power Supply furnishing ±15V and - 5V completes the DVM Analog Block section.

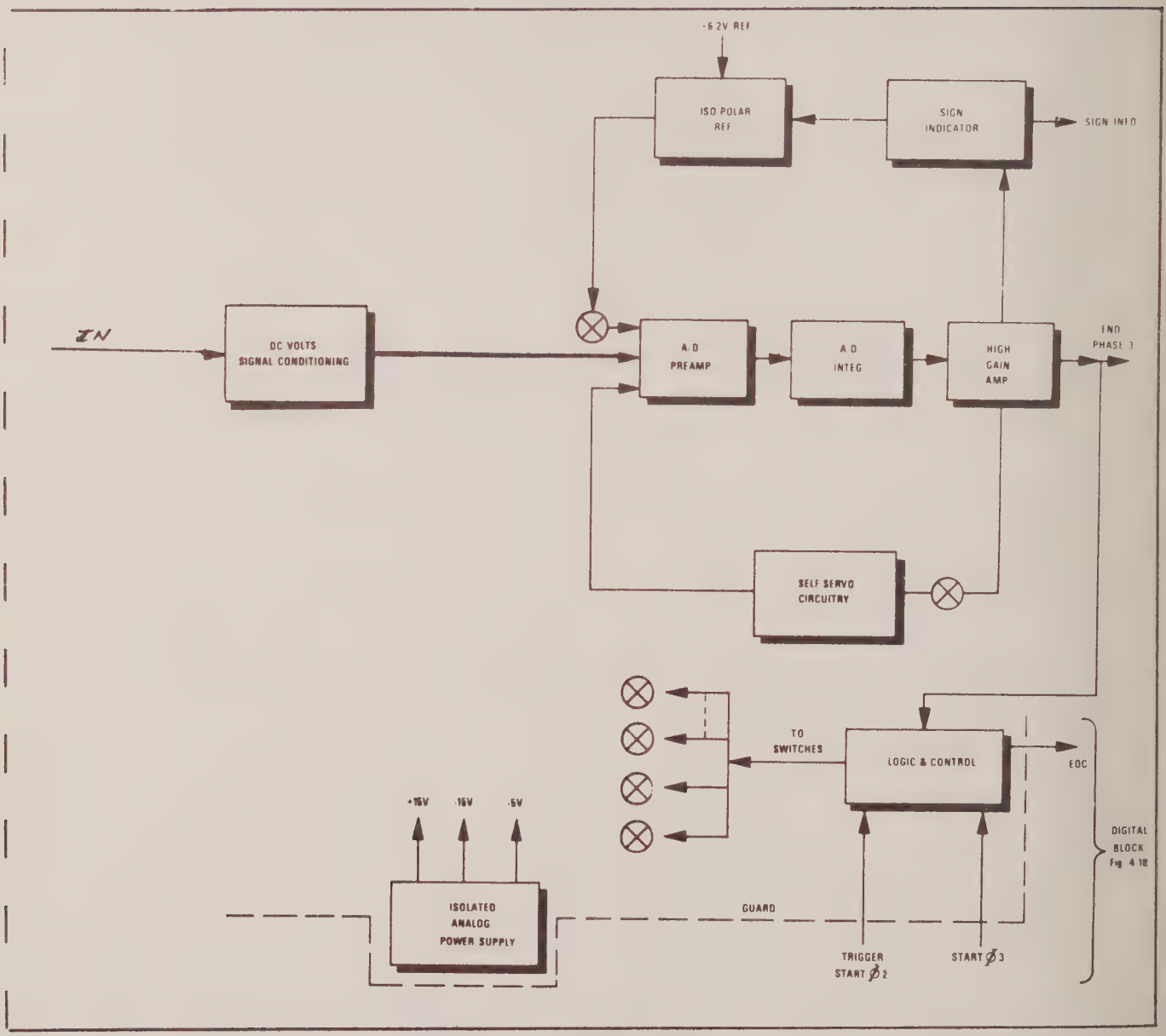


Figure 4-2. Analog Block diagram

b) In the Digital Block Diagram (Figure 4-3), the Trigger Block generates a control pulse (from its own internal timing circuitry or from external command) as the "start convert" command to the Enable FF. If not blocked by the External Enable signal, the Enable FF gate permits the Crystal Clock pulses to drive the Decade Counter Chain block to start phase 2 operation. At 100000 counts (end of phase 2) a carry pulse (10^5 CARRY) is transmitted to the Analog Block to start phase 3, while the decade chain continues its counting. When an EOC pulse is received from the Analog Block, the digital control block applies a stop command to the Enable FF stopping the count. At the same time, the Control Block generates a transfer command to enable the transfer from the Counter to the Latches, Decoders, and Drivers, updating the 5-½ digit display. The updated count (at end of conversion) is held in the Latch and the Display until the next updated count (at end of conversion) is held in the Latch and the Display until the next update and is also available as BCD output

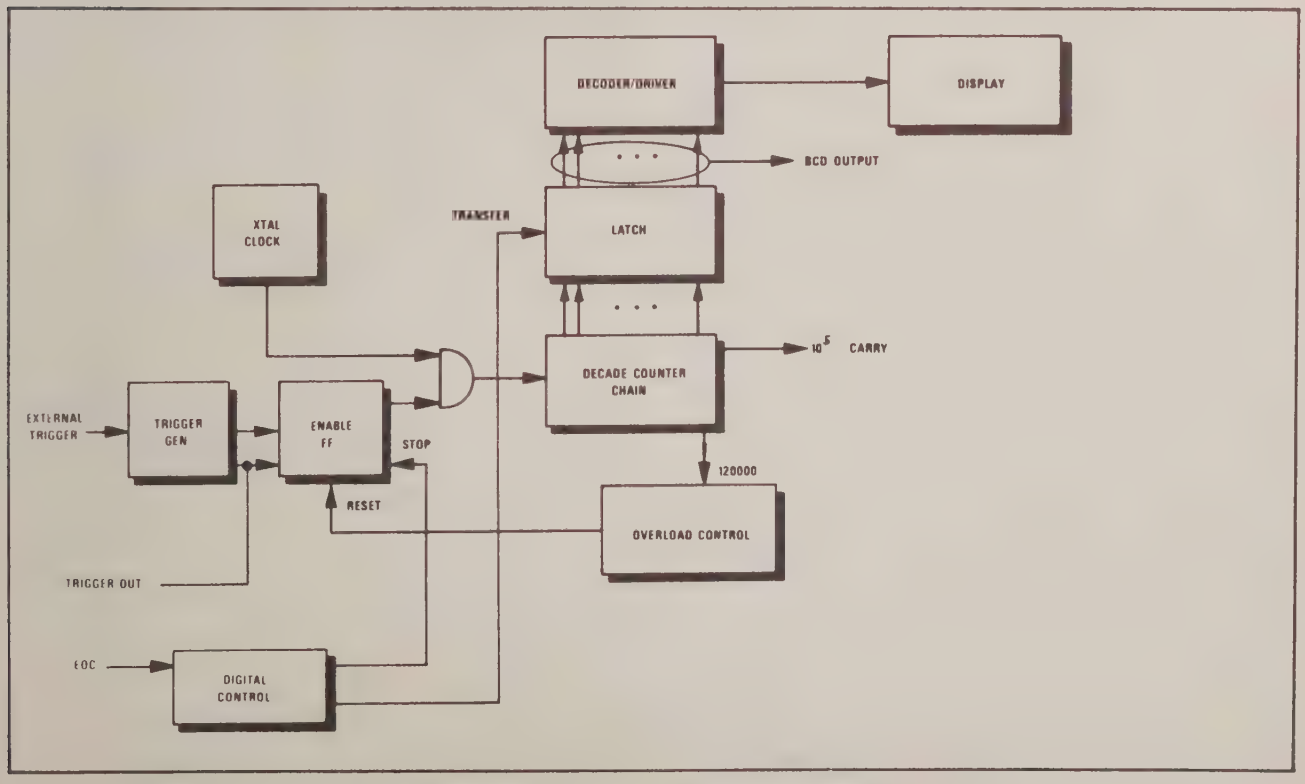


Figure 4-3. Digital Block Diagram

from the Latch Block for remote data output applications.

Paragraphs that follow now trace the signal through the functional blocks of Figures 4-1, 4-2, and 4-3.

3.2 SIGNAL CONDITIONING

An input signal to be measured is introduced into the Signal Conditioning block where it is attenuated for Models 3503, 3504, and 3505, so that a normalized full scale value of ±1.0 volts DC is delivered to the A/D Converter Block. A direct connection is all that is needed for Model 3502, while amplification is introduced for Model 3501 in the A/D converter block. Overrange capability of 120% of full scale is obtained by assuring the accurate operation of the Signal Conditioning block to an output value of ±1.2 volts.

3.3 TRI-PHASIC A/D CONVERTER BLOCK (Figure 4-2)

The three phases of performance of the TRI-PHASIC A/D Converter are:

Phase 1: Accumulation and storage of offset

Phase 2: Integration of Input minus offset

Phase 3: Integration of Reference minus offset

In Phase 1 ---

a. Inputs are disconnected from the A/D Converter:

b. Amplifier is clamped;

c. Long-term non-zero offsets are servo-accumulated and stored for later use;

d. Offset is updated continuously until the DVM phase 1 action ends in response to the trigger command.

In phase 2 ---

a. Clamp is removed and input is connected to the amplifier;

b. Integration of input signal, algebraically reduced by the stored offset value, proceeds for 100 milliseconds as determined by Crystal Clock;

c. Result of the 100-millisecond integration appears as a voltage of the integrating capacitor.

In phase 3 ---

a. Input is disconnected from A/D;

b. Voltage of opposite polarity is selected from ISO-Polar reference, algebraically reduced by value of stored offset, and the difference integrated to discharge the integrating capacitor linearly to zero;

c. At the zero crossover, end of conversion is generated, and transmitted to digital control circuitry.

3.4 TRIGGER GENERATOR AND CLOCK (Digital Block Diagram, Figure 4-3)

Primary control for DVM measurement is the trigger which initiates each conversion (start of phase 2). The trigger, in its internal DVM circuitry is generated by the breakdown of a unijunction transistor after an RC-charge path has charged a capacitor to the breakdown voltage. The trigger is factory selected for a pulse repetition rate of approximately 3 per second.

The trigger may be blocked and a conversion cycle delayed indefinitely by a DTL/TTL low level signal or grounding the ENABLE input for as long as desired. The display, or BCD equivalent, is held until a new trigger is generated.

3.5 DECADE COUNTER CHAIN, LATCH, AND DECODER (Digital Block Diagram)

The decade counter chain, latch, and decoder are composed of monolithic IC units (one for each of five decimal digits in each of the counter, latch, and decoder blocks) under control of digital control flip flops.

During phase 2, the counter fills up to 99,999, and the 5th decade carry pulse switches the actions of the Analog block from phase 2 to phase 3 operations.

During phase 3, the counter continues counting until it is stopped by digital control initiated by the EOC (end of conversion) pulse from the A/D Converter block.

The digital control also enables the transfer from decade counter chain to the Latch which acts as an isolating circuit and storage memory. The BCD data are connected to decoder drivers where they activate appropriate decimal lines in the display components.

3.6 POWER SUPPLY BLOCK

The Power Supply block may be connected for either a 115-volt or 230-volt AC Source of frequency from 47 to 420 Hz. The block is essentially two separate sets of supplies, driven from the same input transformer primary. The analog supply is triple shielded, floating, and incorporated in a "guarded" area for proper isolation. It develops ±15V regulated supply voltage for the analog circuitry, -5V for the digital control in this section, and develops the 6.2 volt, oven controlled, extremely low temperature coefficient, reference source for the A/D Converter. Common ground for the precise reference is used as the high voltage for the isolated digital control section, where the low voltage level is the -5 volts.

The transformer primary drives three additional secondaries whose outputs are rectified and provide +180 volts for display operation, and a regulated +5 volts for digital logic. These appear in the digital section of the converter, and use the digital ground as their return.

3.7 DETAILED OPERATION

A more complete function diagram of the voltmeter is illustrated in Figure 4-4. The major blocks comprising the unit are divided into subunits or are repeated to indicate the several functions performed sequentially by the block, and this division forms a basis for complete systems understanding, detailed circuit explanation, and maintenance. Complete schematics, from which simplified schematics and block diagrams have been derived, are included at the back of the book.

The sequence of functions illustrated in Figure 4-4 consists of the following:

a) Proper attenuation elements for the particular model of the Series 3000 DVM perform the necessary scaling in the Signal Conditioning block.

b) Prior to the trigger pulse starting a conversion measurement, the A/D Converter input is clamped, and the Signal Conditioning output is removed from the A/D Converter. During that time, phase 1 drift integration proceeds and the self zeroing circuit determines the A/D amplifier accumulated drift and stores it for phase 2 and phase 3 operation.

c) Following the trigger pulse generated in the Timing & Control unit;

1) The clamp is removed from the A/D Converter.

2) The Signal Conditioner Output is connected to the input of the A/D Converter.

3) The self-zeroed drift is introduced as an algebraic negative offset.

4) The counter is reset to zero and starts its fixed count for the phase 2 integration.

d) When the count has reached 100000 (100 millisec.),

1) The second integration is stopped.

2) The sign of the input is interrogated by strobing the integrator output.

3) The unknown signal input is removed from the integrator.

4) The appropriate polarity of internal reference voltage is applied to the A/D input.

5) The reference voltage reduced algebraically by the stored drift (as in phase 2) is integrated during phase 3 integration.

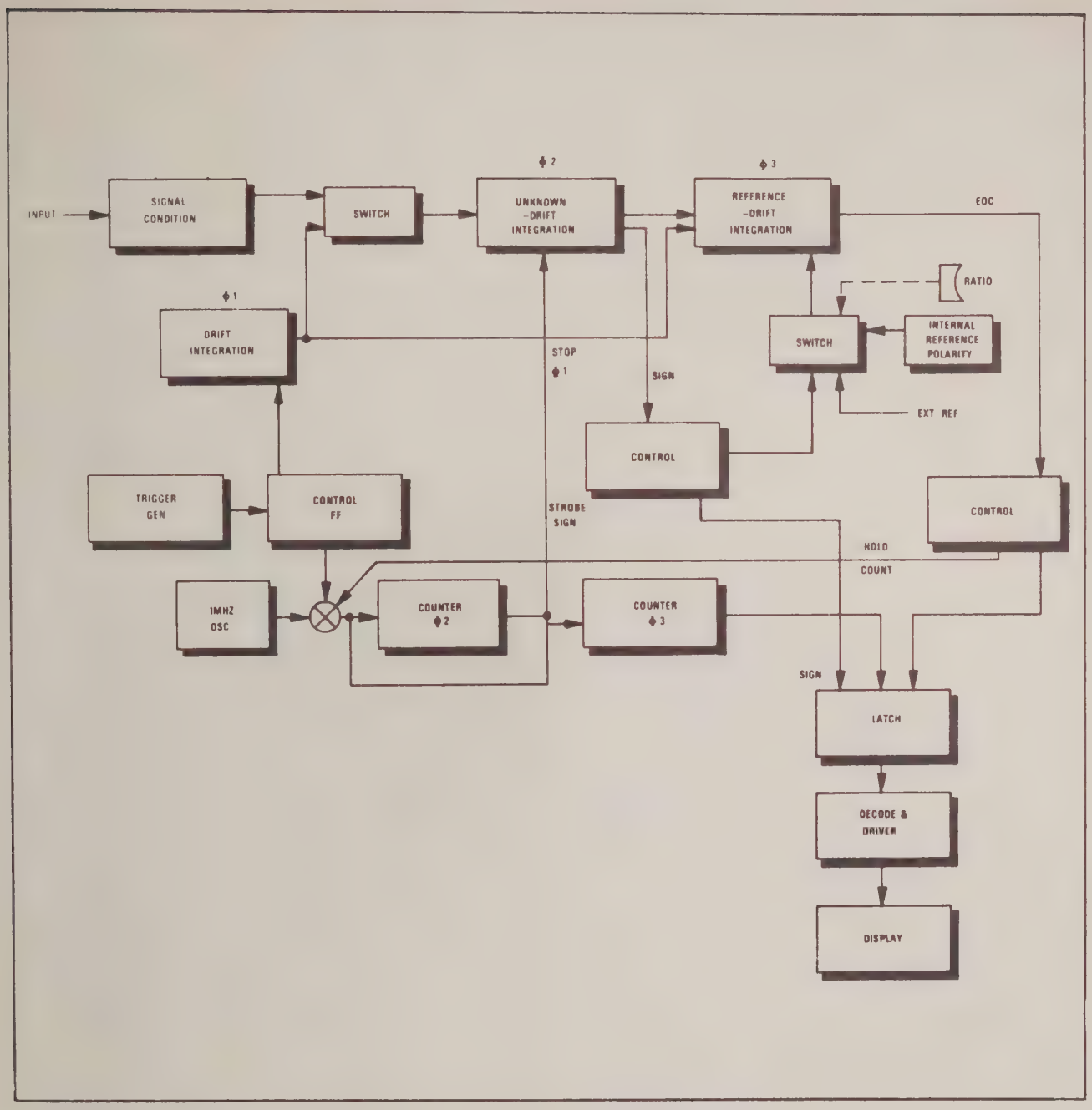


Figure 4-4 Functional System Block Diagram

e) When the integrated reference compensates the integrated unknown input (when the output of the integration returns to the starting point),

1) Phase 3 integration process ends.

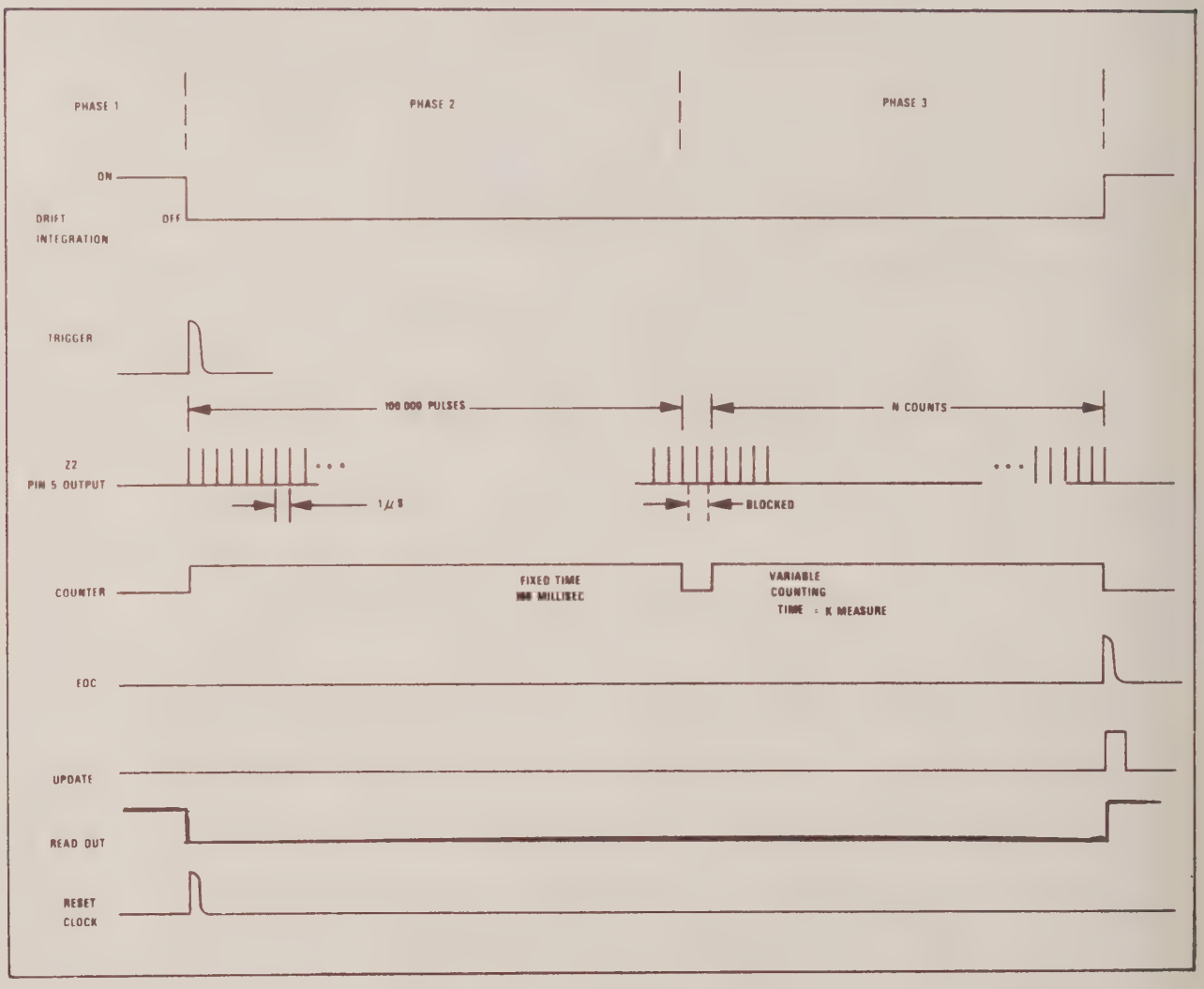


Figure 4-5. System Timing Diagram

2) The input clamp is reestablished.

3) The clock input to the counter is stopped.

4) A READ OUT signal is transmitted indicating End of Conversion.

5) The accumulated count is transferred to the display.

The timing sequence is illustrated in the chart of Figure 4-5, indicating the three phases of the operation.

3.8 A/D CONVERTER DETAILS

Operation of the Tri-Phasic A/D Converter in its 3 phases is described with the aid of simplified schematics of Figure 4-7A and Figure 4-7B, derived from the complete reference drawing.

Referring to Figure 4-7A, during phase 1, switch Q1 is open, switches Q2, Q23, and Q25 are closed. Opening of Q1 removes the Signal Conditioned input from the A/D preamplifier A1. Closing of Q2 clamps the input to A1, and, with Q23, closes a path whereby C34 is charged from the ISO-Polar reference to 1 volt. Closing of Q25 permits capacitor C36 to store a charge compensating for the accumulated non-zero offset in A1, A2, and Z29.

Appearance of the trigger pulse in the secondary of transformer T2(Figure 4-7B) signals the start of phase 2, and initiates the control actions by flip flop Z31A. The trigger causes pin 5 to go high and consequently Q1 to close. The output Z31A pin 8 goes low, and consequently opens transistor switches Q2, Q23, and Q25.

a. Opening Q23 opens the charging path to C34 (Figure 4-7A) and leaves C34 charged to 1 volt and isolated during phase 2.

b. Opening Q25 opens the charging path of C36 and leaves it charged with the accumulated compensation for zero drift applied to the input of the differential integrating amplifier A2.

c. Closing Q1 connects the Signal Conditioned output to the A/D Converter input.

Phase 2 integration action takes place in the chain of three active elements: amplifier A1, amplifier A2, and amplifier Z29. Amplifier A1 is a high gain, high input impedance, low offset amplifier whose feedback resistors R93 and R94 determine the closed loop gain.

The output of amplifier A1 is one input to integrating amplifier A2 whose integration constant is determined by C35 and R95. The other input to amplifier A2 is the voltage on C35, the stored value of the voltage compensating for the accumulated zero offset derived in phase 1.

Output of amplifier A2 drives high gain amplifier Z29 to saturation during phase 2. Its output polarity is used to indicate the sign of the unknown input.

Phase 2 integration proceeds until the appearance across the secondary of T4 of a positive-going pulse signalling a 10^5 carry from the digital block. This now appears as a negative pulse clocking flip flop Z30A pin 2 and as a direct set for flip flop Z31A (pin 4). The resulting actions controlled by these flip flops initiate the phase 3 operation of the A/D Converter.

The output, pin 5, of Z31A, which had been high from the start of phase 2, now goes low opening Q1 thereby removing the signal input from the A/D amplifier. Action of flip flop Z30A in response to the clocking pulse depends upon its input conditions just prior to receiving that pulse. This in turn was determined by the output

of amplifier Z29 during phase 2. Amplifier Z29 was driven to saturation in the positive or negative direction corresponding to the sign of the input signal.

If the input signal had been positive, Z30A pin 11 would have been low and the clocking pulse would not have changed the high level at pin 6, thus producing no pulse across the primary of "sign" pulse transformer T5. If the input signal had been negative, Z30A pin 11 would have been high and the clocking pulse would cause Z30A pin 6 to go low producing a pulse across the transformer T5 primary and transmitting a negative sign indication to the Digital circuitry. The voltage level developed by flip flop Z30 at pin 9 controls the sign of the reference signal to be switched to the amplifier input at the start of phase 3. (Refer to Figure 4-8 in conjunction with Figure 4-7B).

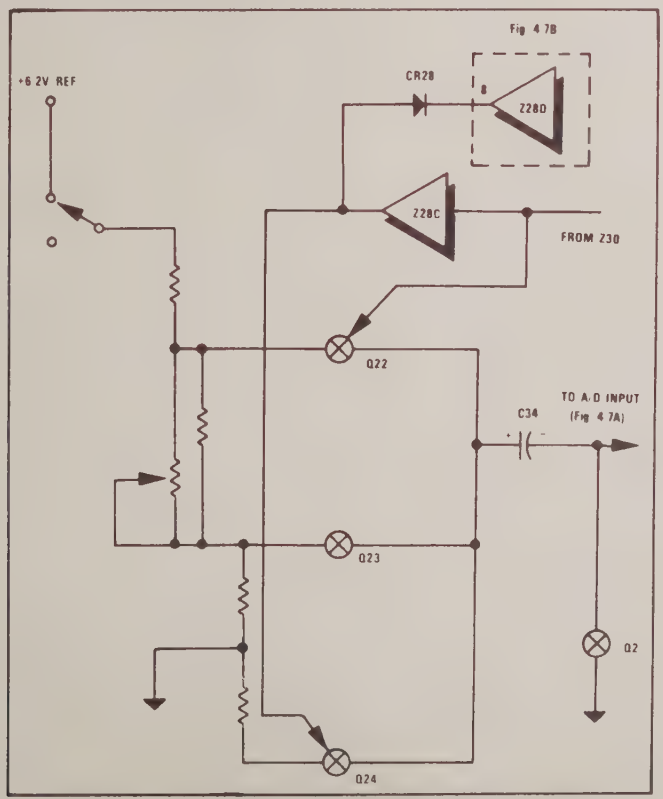


Figure 4-8 ISO-Polar Reference Switching Simplified Schematic

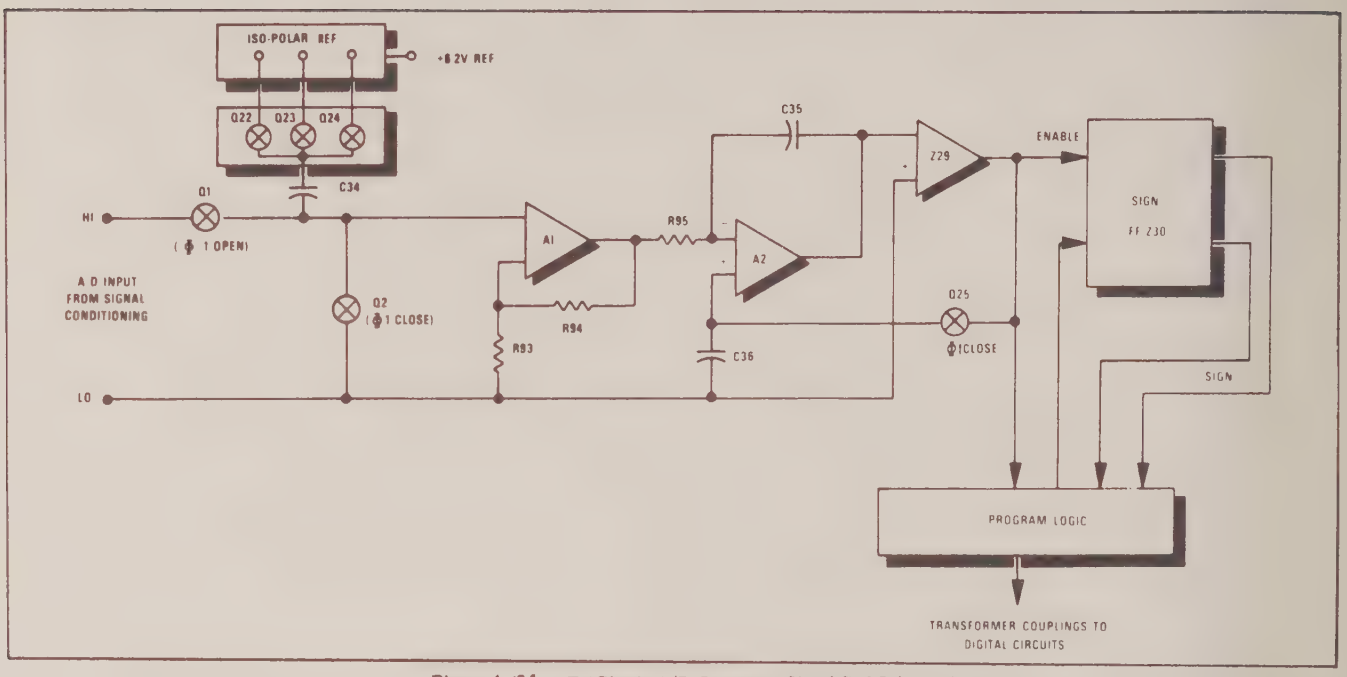


Figure 4-7A. Tri-Phasic A/D Converter Simplified Schematic

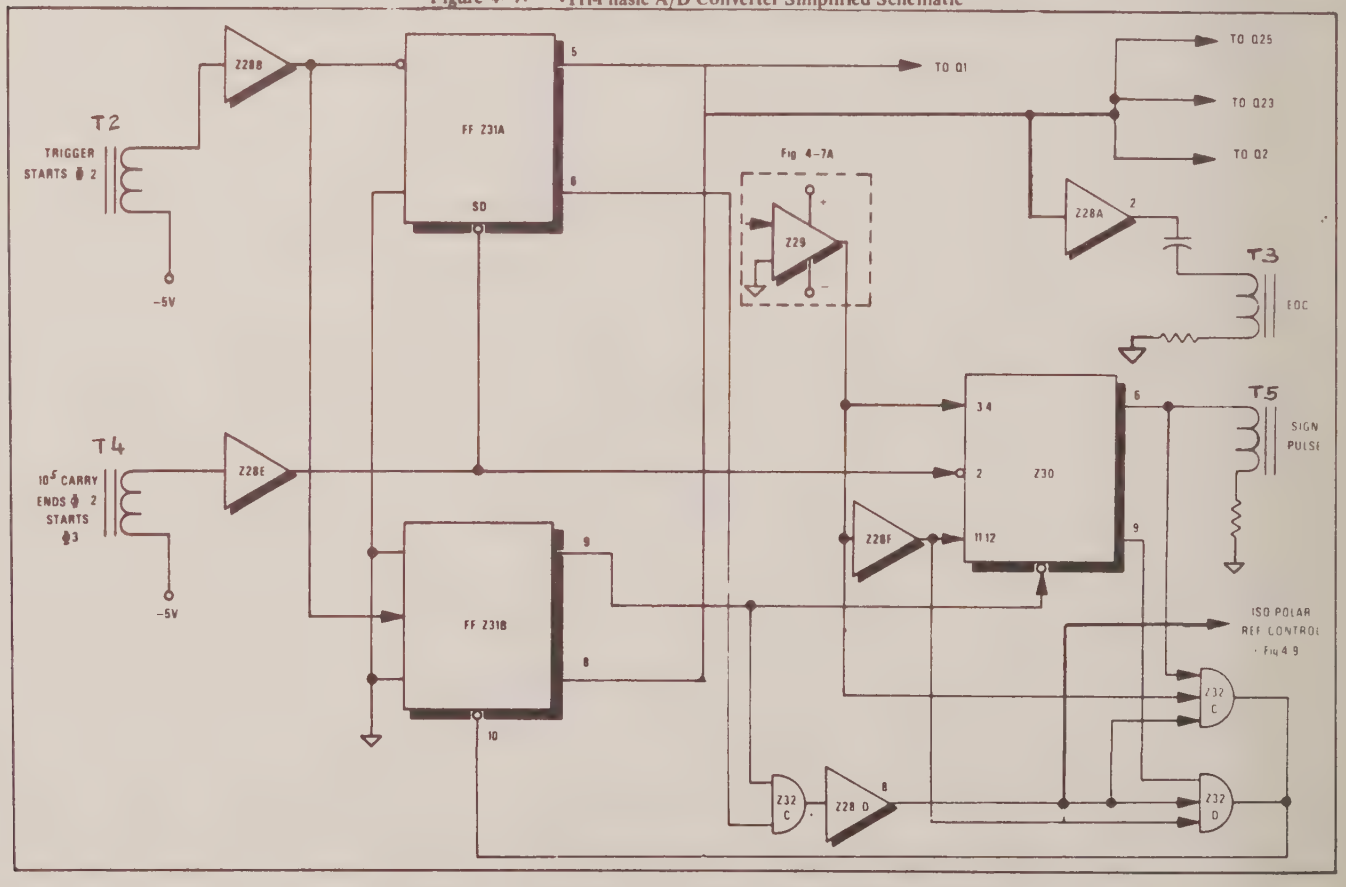


Figure 4-7B. Tri-Phasic A/D Converter Control Simplified Schematic

During phase 2, both Q22 and Q24 are open. The low level output at Z30 pin 9 had kept Q22 open; and the output of Z28 pin 6 had been clamped low through CR28 to Z28D, keeping Q24 open. If the input signal had been positive, Z30 pin 9 would have remained low, keeping Q22 open. The carry pulse control action removes the clamp on the Z28 pin 6 output permitting the output of Z28 pin 6 to go high, closing Q24. This action places the high side of C34 at reference zero potential and negative, Z30 pin 9 would go high, closing Q22 and connecting the high side of C34 to reference +2V causing a positive one volt at the A/D amplifier input.

Control actions for the end of conversion (end of phase 3) are initiated by the zero crossing of the Z29 output, sensed by the gating action of Z32C and Z32D, and developed in digital control flip flops Z31. At each gate Z32C and Z32D, two of the three inputs are high during phase 3. As the output of Z29 crosses zero in either direction, one of these gates is enabled and develops the negative direct set pulse at flip flop Z31 pin 10. The Z31D output goes high, is inverted by Z28A, and develops a pulse across EOC transformer primary, signalling end of conversion to the digital circuitry. The Z31D output also controls the resetting of A/D converter to phase 1 operation. It --

a. Closes Q25

b. Closes Q2

c. Clamps Z28 pin 6; opens Q24

d. Direct sets Z30; opens Q22

e. Closes Q23

f. Opens Q1.

In summarizing the actions of the A/D converter circuitry during the three phases of operation, the levels and signals of the gates, flip flops, etc. are tabulated below. (Next Page)

3.9 TRIGGER GENERATOR AND COUNTER

3.9.1 Trigger Generation

The trigger pulse initiating each conversion process may originate either from an external source or from internal circuitry shown in the simplified from of Figure 4-9. Capacitor C1 charges toward +5V through R15 until the firing voltage of Q40 is reached. A pulse approximately 100 usec wide and 4 volts magnitude is developed across the resistor R16 and connected to the J input of the control flip flop Z2 pin 2. The saw-tooth charge-discharge signal and the resulting timing signal waveforms are shown in Figure 4-9.

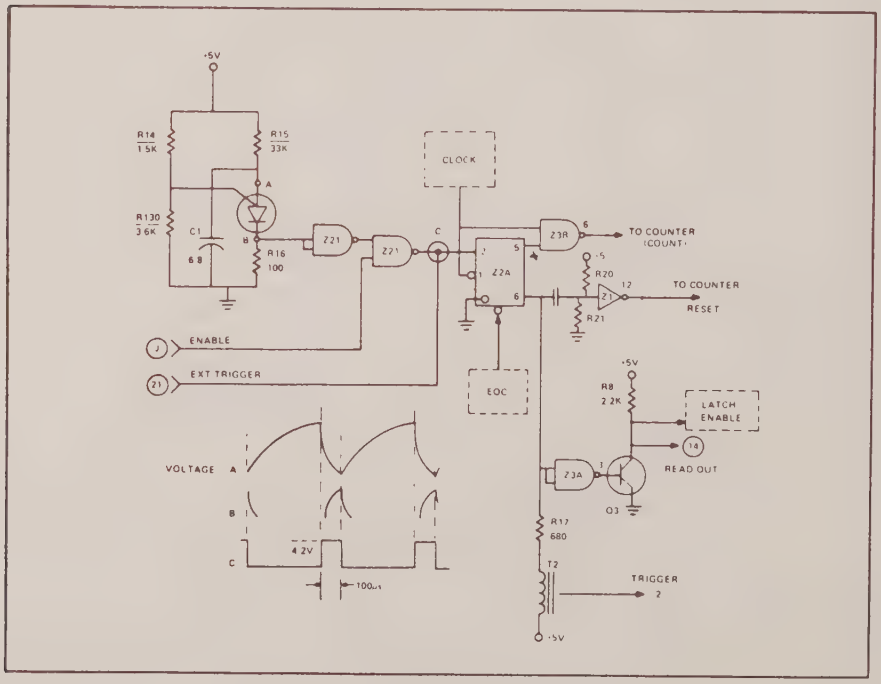


Figure 4-12 Trigger and Timing Generator

LOGIC LEVELS

ACTION	Z	PIN	LEVEL
INITIAL CONDITIONS Ø1	Z31	1	High
		2	High
		4	High
		5	Low
		6	High
		8	High
		9	Low
		10	High
	Z30	10	Low
		3	High
		6	High
		9	Low
		11	Low
	Q1		Open
	Q2		Closed
	Q22		Open
	Q23		Closed
	Q24		Open
	Q25		Closed
	Z28	8	Low
Ø2 STARTS WITH POSITIVE PULSE THROUGH T2	Z31	1	Clock pulse
		13	Clock pulse
		5	High
		6	Low
		8	Low
		9	High
	Z30	10	High
	Z28	8	Low
	Q1		Closed
	Q2		Open
	Q22		Open
	Q23		Open
	Q24		Open
	Q25		Open
Ø3 STARTS WITH CARRY PULSE THROUGH T4	Z31	4	Neg. pulse
		6	High
		5	Low
	Z30	2	Clock pulse
		3	High if input pos. Low if input neg.
		11	Low if input pos. High if input neg.
		6	High if input pos. Low if input neg.
		9	Low if input pos. High if input neg.

ACTION	COMP	PIN	LEVEL
	T5		Pulse if input neg. No pulse if input pos.
	Z28	8	High
	Q1		Open
	Q2		Open
	Q22		Closed if input neg. Open if input pos.
	Q23		Open
	Q24		Open if input neg. Closed if input pos.
	Q25		Open
END OF Ø3; Z29 PIN 7 CROSSES ZERO	Z32	6 or 8	Goes neg. pulse
	Z31	10	Low
		8	High
		9	Low

ACTION	COMP	PIN	LEVEL
END OF CONVERSION; NEGATIVE PULSE THROUGH T3	Z30	10	Low
		6	High
		9	Low
	Z32	8	High
		6	High
	Z28	8	Low
	Q1		Open
	Q2		Closed
	Q22		Open
	Q23		Closed
	Q24		Open
	Q25		Closed
RETURNING TO Ø1 OPERATION			

With the trigger pulse enabling Z2A, the next clock pulse toggles Z2. Pin 5 goes high and pin 6 goes low providing a control output with the following results:

1. After inversion through Z3 pin 3, transistor Q5 conducts; its collector goes low isolating the latching circuit from the counter. The latch and display retain the stored count until the next conversion update, and an output signal, READOUT, is available at the rear panel connector to indicate this event in the cycle. This is a High (T^2L/DTL) output level between conversions.

2. The leading edge of the negative going waveform is differentiated (C5, CR20, and R21) as the input to Z1 (pin 13), inverted, and generates a positive going pulse to reset the decade counter IC's, Z4 through Z8.

3. The inverted counter reset pulse, at the output of Z1 (pin 10) presets the control flip flops Z20 pin 10, and pin 4, and Z2 pin 10.

4. Z3 pin 4 is enabled, allowing the clock to drive the counter through the gate Z3B pin 6.

3.9.2 Counter Chain

The crystal-controlled clock is a series-mode crystal circuit consisting of crystal Y1 and inverter Z1. It develops 1 MHz pulses which are gated into the counter during phases 2 and 3. The counter registers accumulate the count during phases 2 and 3 until receipt of the EOC (End of Conversion) pulse at the EOC transformer secondary. This resets flip flop Z2, and pin 5 goes low, blocking the timing

pulses at gate Z3 (4, 5, 6). Simultaneously, Z2 pin 6 goes high cutting off Q5, collector voltage goes high, permitting the count in Z4-Z8 and Z2 to be transferred to the latches, and through them to the decoding and display driving registers Z15 and Z19.

Outputs of the counter chain are transferred through the latching registers as BCD data. These are immediately available at the tab connector of the DVM rear panel for remote display or control purposes. In the DVM, the decoding registers Z1 through Z6 (in the display), convert BCD to decimal signals for their respective digits.

3.9.3 Overload

If an end of conversion pulse is not received during phase 3 by the time the counter reaches 120000 (a display of 120000), an OVERLOAD condition exists, and this event is sensed at gate Z3. One input to Z3 (pin 9) is set at a high level by the toggled output of Z20 pin 5 when the count reaches 10^5 in phase 3. When the counter reaches 20000, the second input to Z8 (pin 10) goes high and activates the gate. The gate output, Z3 pin 8 is a negative waveform, available at rear panel connection, pin Y, as an OVERLOAD indicating signal for remote transmission. The overload indicating negative level also is connected at the output of Z1 pin 2 and acts in the same way as the EOC pulse from the Analog Circuitry through Z11 pin 2 as a direct set for flip flop Z2 pin 4.

The overload condition, generating high levels of 10^5 and 2×10^4, back bias CR47 and CR46, respectively, and the combined

action cuts off transistor Q2 to turn off the digit indicator (MSD-1) of the most significant digit in display tube DS2. At the start of the next conversion cycle, when the counter is reset, the back bias levels are removed, and the display responds to the 10^5 count to turn DS2 on during the conversion. Thus, the most significant digit blinks as a result of successive overload conditions.

3.9.4 Sign

DS1 is the display unit for the sign indication. It is turned on by the action of the sign pulse transformer T5 output via latch flip flops Z14, and strobed into first latch at carry pulse and transferred to second latch at EOC.

Chapter 4

CALIBRATION & MAINTENANCE

4.1 GENERAL

Each Series 3500 Digital Voltmeter has been calibrated at the factory with standards traceable to the National Bureau of Standards, and should remain within calibration under normal operating conditions for periods of six months or more. When recalibrating the instrument, test standards of the accuracy shown below should be used, and the step-by-step procedures performed in the sequence shown.

Access to calibrating adjustments is provided through holes in the guard over the analog section. Do not remove this guardshield, and use an insulated tool when making the adjustments.

Note: Allow one hour warm-up before calibrating.

4.2 TEST STANDARD REQUIRED

COHU MODEL 355, or equivalent.

DC Volts

Model 3001	.1V ± .001% rdg ±2uV
Model 3002	1V ± .001% rdg ±2uV
Model 3003	10V ± .001% rdg ±5uV
Model 3004	100V ± .001% rdg ±20uV
Model 3005	1000V ± .001% rdg ±40uV

4.3 STEP-BY-STEP CALIBRATION

Perform the adjustments in the following sequence:

I. DC Voltage Calibration

(a) zero adjust of current and voltage (for Models 3501, 3503, and 3505)

(b) balance adjust

(c) full scale reading adjust

II. Ratio Calibration for models equipped with Option 1, 2, 3, or 4. The procedure for each model follows:

4.4 DC VOLTAGE CALIBRATION

4.4.1 Model 3501

(a) Zero adjust

1. Connect shorting bar across Vx terminals
2. Adjust R300 for a display of ± 000000.

4.4.2 Model 3503

(a) Zero adjust

1. Connect 10 Meg across input Vx
2. Adjust R45 for ±00.0000 display
3. Connect shorting bar across input Vx
4. Adjust R46 for ±00.0000 display
5. Repeat steps 1-4 as necessary.

4.4.3 Model 3505

(a) Zero adjust

1. Connect shorting bar across input Vx.
2. Adjust R46 for ±0000.00 display.

4.5 ALL MODELS BALANCE ADJUST

1. Apply + full scale to input Vx.
2. Read display. Record.
3. Reverse input polarity. Read display.
4. Adjust R83 until values of 2 and 3 are exactly equal.
5. Repeat steps 1 - 4 as necessary.

4.6 ALL MODELS FULL SCALE ADJUST

1. Apply full scale to input Vx.
2. Adjust R87 for display of full scale.

4.7 ALL MODELS RATIO ADJUST

1. Select ratio mode.
2. Apply full scale to input Vx.
3. Apply +10.0000V to input Rx.
4. Adjust R86 for display of full scale.

4.8 MAINTENANCE

4.8.1 General

Should the meter need repair while within the warranty period, it should be returned to the factory for appropriate action. Damage while attempting repairs, or misuse resulting in instrument damage may invalidate the warranty.

4.8.2 Trouble Shooting

If the meter cannot be calibrated, or is otherwise malfunctioning, the trouble may be isolated by using the diagnostic program suggested by the routines of Diagrams 32-3020 and 32-3022. These routines should be followed after all power supply voltages have been verified. See the power supply schematic, 35-1013. Consult the previous chapter, Principles of operation, to support the troubleshooting analysis.

Replacement exlectronic parts are listed in the following pages.

PARTS LIST

23-111002	CAP CERM 12PF 10% 1KV	1	C49
23-111003	CAP CERM 5PF	4	C46/50
23-111004	CAP CERM 30 10% N150	1	C7
23-111005	CAP CERM .001UF 10%	3	C3/5/58
23-111006	CAP CERM .01UF 150V	1	C47
23-118010	CAP CERM .005UF GMV 1.6KV	2	C201/202
23-310002	CAP MICA 10PF 5% DM10	3	C1/3/4
23-310023	CAP MICA 100PF 5% DM10	1	C2
23-311003	CAP MICA 20PF 5% DM15	1	C15
23-311022	CAP MICA 270PF 5% DM15	2	C2/75
23-311038	CAP MICA 1500PF 5% DM15	1	C4
23-441003	CAP TANT 15UF 20% 10V	8	C5/6/36/44/48/205/206
23-441005	CAP TANT 6.8UF 20% 20V MIN	9	C1/18/19/39-43
23-510002	CAP PC 2UF 10% 50V AX	4	C34
23-550103	CAP PSTY 3000PF 30V AX	1	C300
23-550104	CAP PSTY .68UF 10% 50V AX	1	C35
23-550105	CAP PSTY .018UF 10% 50V AX	1	C45
23-620004	CAP AL EL 4.7UF 315V	1	C52
23-620005	CAP AL EL 2500UF 15V	1	C204
23-620007	CAP AL EL 330UF 50V	1	C38
24-100021	DIODE 300V BRIDGE KBP04	3	CR201/202
24-104004	DIODE RECT 1N4004	5	CR30-34
24-110001	DIODE 1N4148	30	CR1/2/3/4/5/7-20/22-28/29/36/44
24-120002	DIODE ZENER IN702A	1	CR6
24-120075	DIODE ZENER 1N752A	2	CR35/213
24-121008	DIODE ZENER IR180B	1	CR38
24-130004	DIODE REF 1N829 SEL 8-1054	1	CR37
24-203440	TRANS PWR NPN 2N3440	1	Q10
24-206027	TRANS UJT-SCR 2N6027	1	Q40
24-220314	TRANS PWR NPN 40314	1	Q19
24-220319	TRANS POWER 40319	2	Q18/20
24-225296	TRANS POWER 2N5296	1	Q201
24-234410	TRANS GP NPN 2N4410	8	Q1/2/4-9
24-405558	IC 5558V LIN DIL MINI	1	Z33
24-420311	IC 311H LIN TO-5 8 PIN	1	Z29
24-469094	IC 9094 DTL DIL	4	Z2/20/31
24-469937	IC 9937 DTL DIL	2	Z1/28
24-469948	IC 9948 DTL DIL	3	Z30
24-469949	IC 9949 DTL DIL	2	Z3/21
24-469962	IC 9962 DTL DIL	1	Z32
24-A07475	IC 7475	6	Z27/9-14
24-A07490	IC 7490	5	Z4-8
24-A08880	IC 8880	6	Z1-6
25-100002	INDUCTOR 220 UHY	2	L201/202
25-100101	INDUCTOR 100UHY (48-1051)	1	L1
25-210351	DISPLAY SP351	1	DS1
25-210352	DISPLAY SP352	1	DS2
25-210353	DISPLAY SP353	1	DS3
25-501003	FUSE 1/2A SLO BLO	1	F201
27-230153	RES NETWORK 899-3-R15K	1	A1
27-230222	RES NETWORK 899-3-R2.2K	1	A2
36-1056	TRTANSFORMER ASSY(TOROID)	1	T2-5
38-1002P1	TRANSFORMER	1	T1
38-1007-1	RES SET	1	R81/84/85/89
38-1012	CRYSTAL 1 MHZ	1	Y1
48-1014B-A	TRANS FET SEL BLUE	2	Q22/23

PARTS LIST

22-021019	RES 100 1/4W 5% CC	7	R16
22-021029	RES 1K 1/4W 5% CC	9	R7/13/21/201
22-021059	RES 1MEG 1/4 5%CC	1	R111
22-021529	RES 1.5K 1/4W 5% CC	4	R120
22-022229	RES 2.2K 1/4W 5% CC	14	R1/8-10/24-28/98/109/118
22-022239	RES 22K 1/4W 5% CC	1	R12
22-022269	RES 22MEG 1/4W 5% CC	1	R5
22-023329	RES 3.3 K 1/4W 5% CC	7	R4/19/21/23/107
22-023339	RES 33K 1/4W 5% CC	2	R15/92
22-023369	RES 33MEG 1/4W 5% CC	1	R33
22-023629	RES 3.6 K 1/4W 5% CC	1	R130
22-025149	RES 510K 1/4W 5% CC	6	R114
22-026819	RES 680 1/4W 5% CC	4	R2-7/122
22-028239	RES 82K 1/4W 5% CC	1	R13/17/100/101
22-029129	RES 9.1K 1/4W 5% CC	1	R6
22-031019	RES 100 1/2 W 5% CC	1	R108
22-065139	RES 51K 4W 5% CC	2	R117/127
22-331052	RES 10.5K 1% RN55D	1	R104
22-331432	RES 14.3K 1% RN55D	1	R8
22-331502	RES 15.0K 1% RN55D	3	R47/48/96
22-331503	RES 150K 1% RN55D	2	R95
22-332742	RES 27.4 1% RN55D	1	R1
22-333011	RES 3.01K 1% RN55D	1	R2/3/99
22-333012	RES 30.1K 1% RN55D	2	R2/3
22-337151	RES 7.15K 1% RN55D	1	R9
22-341002	RES 10K 1% RN55C	4	R106
22-346191	RES 6.19K 1% RN55C	1	R105
22-348661	RES 8.66K 1% RN55C	1	R103
22-362613	RES 261K 1% RN60D	1	R50
22-371101	RES 1.1K 1% RN60C	1	R102
22-392001	RES 1M 1% RN65C	1	R82
22-666101	RES TRIM 100 ZA1012	2	R46/86
22-666251	RES TRIM 250	3	R32/75/87
22-666253	RES TRIM 25K ZA2532	4	R30/38/45/300

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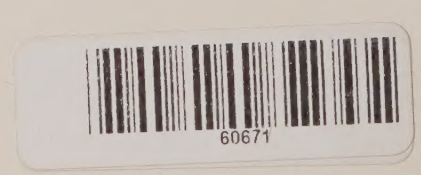

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